Effects of Design, Structure and Material on Thermal-Mechanical Reliability of Large Array Wafer Level Packages

Bhavesh Varia[1], Xuejun Fan[1, 2], Qiang Han[2]
[1]Department of Mechanical Engineering
Lamar University
PO Box 10028, Beaumont, Texas 77710, USA
[2]College of Civil Engineering and Transportation
South China University of Technology, Guangzhou, China
bhaveshvaria.mech@gmail.com; xuejun.fan@lamar.edu

Abstract

In this paper, thermo-mechanical reliability of a variety of state-of-art wafer level packaging (WLP) technologies is studied from a structural design point of view. Various WLP technologies, such as Ball on I/O with and without redistribution layer (RDL), Ball on Polymer with and without under bump metallurgy (UBM) process, and encapsulated Copper Post WLPs, are investigated for their structural characteristics and reliability performance. Ball on I/O WLP, in which solder balls are attached directly to the metal pads on silicon wafer, is used as a benchmark for the analysis. 3-D finite element modeling is performed to investigate the effects of WLP structures, UBM process, polymer film material properties (in Ball on Polymer), and encapsulated epoxy material properties (in Copper Post WLP). Fundamentals underlying thermomechanical reliability mechanisms are uncovered through detailed parametric studies. Experimental tests with various parameters were conducted to validate simulation results. Both Ball on Polymer and Copper Post WLPs have shown great reliability improvement in thermal cycling. Encapsulated copper post WLP showed the best performance.

1. Introduction

Wafer level packaging (WLP) is one of the fastest growing segments in semiconductor packaging industry due to the rapid advances in integrated circuit (IC) fabrication and the demands of a growing market for faster, lighter, smaller, yet less expensive electronic products. Higher performance, low cost compared to die level packaging, and small form factor are three primary advantages of WLP. So it becomes a pioneer in the recently growing market of handheld and mobile electronic systems (Fan *et al.*, 2008, 2009) [1-2].

Thermo-mechanical reliability of wafer level packages is still a major concern because solder joint thermal cycling reliability is the weakest point of technology. In order to withstand against thermal cycling, WLP packages must have relatively smaller die size and I/Os. However, there has been a demand for larger number of I/Os and larger size because of more integrated functionality.

A WLP is basically a chip scale package because the final package is same as die. A typical WLP on board has three major elements: silicon die, solder balls and the printed circuit board. The large difference between the coefficient of thermal expansion (CTE) of silicon (~2.6ppm/°C) and PCB (~17ppm/°C) limits the solder ball thermal cycling fatigue performance. In order to improve the reliability, a variety of WLP technologies have been developed (Fan *et al.*, 2008,Reche *et al.*, Kim *et al.*, 2002)[1][3][4]. There are several materials involved with different WLP structures. Dimensions, structural design, and material properties have great influence on reliability.

In this paper, various state-of-art WLP technologies and the corresponding thermo-mechanical reliability are analyzed from a structural design point of view. These WLP technologies include standard WLP (ball on I/O), WLP with redistribution layer (RDL) and under bump metallurgy (UBM) process (ball on polymer with UBM), WLP with redistribution layer without UBM process (ball on polymer without UBM), as well as encapsulated copper post WLP [6-10]. Detailed structures of each WLP are described. 3-D finite element models are created for various WLP structures. The effects of various WLP structures, UBM process, polymer film material properties (in Ball on Polymer), and encapsulated epoxy material properties (in Copper post WLP) are studied. The following parameters are considered in the study,

1) Different WLP structures
2) Ball pitch effect
3) Redistribution layer geometry effect
4) Redistribution layer material properties
5) UBM effect
6) Array size
7) Solder ball shape
8) PCB design

The simulation results are compared to the experimental test data and failure analysis. The mechanisms in enhancing thermo-mechanical reliability of WLP are discussed.

2. WLP Descriptions

Four different WLP packages, as shown in Table 1, are studied.

Table 1 WLP descriptions

WLP Structures	Descriptions
WLP Structure A	Standard WLP (Ball on I/O)
WLP Structure B	Ball on polymer without UBM
WLP Structure C	Ball on polymer with UBM
WLP Structure D	Encapsulated copper post

2.1 WLP Structure A: Standard WLP

Ball on I/O WLP is a standard wafer level packaging technology and the process is very similar to a typical flip chip technology. As shown in Figure 1, the ball is attached to the aluminum pad directly through under bump metallurgy (UBM). The bumps are directly attached to the final I/O metal pad. Passivation opening, overlapped by UBM, provides a seal to the under laying I/O aluminum pad. The solder ball in this structure is connected to silicon base directly. Figure 2 is a schematic view of details of WLP Structure A.
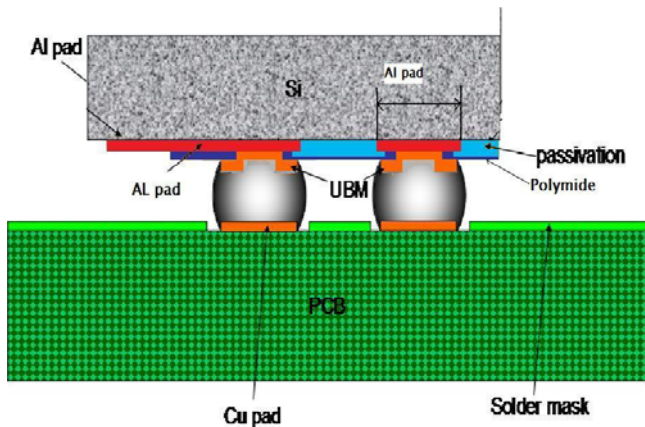

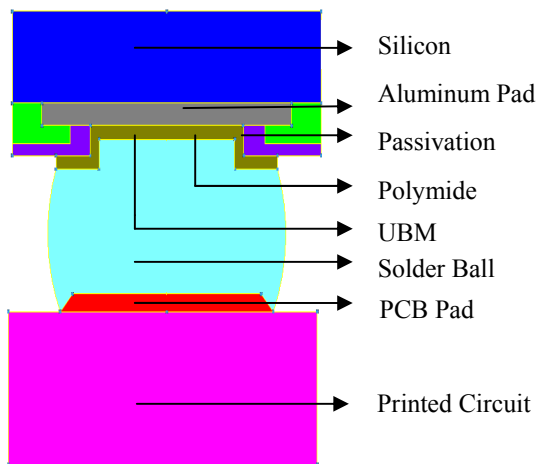Figure 1 WLP structure A-Standard WLP

Figure 2 A schematic cross section view of bump structure for WLP Structure A

2.2 WLP Structure B: Ball on Polymer without UBM

Figure 3 shows a schematic diagram of ball on polymer without UBM. Redistribution traces and pads are usually processed with electroplating using copper, which makes it possible to attach solder balls directly on RDL pads without UBM. Detailed structure is shown in Figure 4. Solder balls in this structure sit on a dielectric polymer film layer to avoid a direct connection with silicon base.
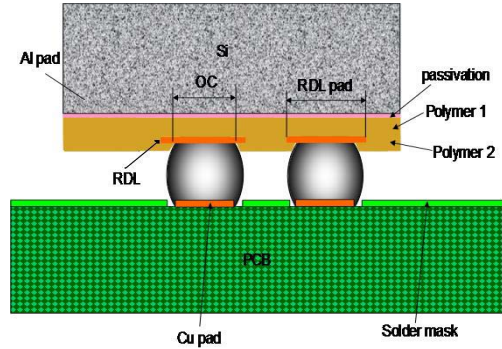

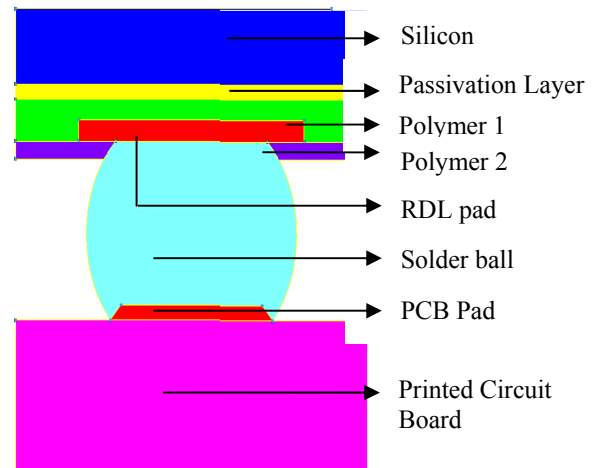Figure 3 A schematic diagram of WLP Structure B-Ball on Polymer without UBM

Figure 4 A schematic cross section view of bump structure for WLP Structure B

2.3 WLP Structure C: Ball on Polymer with UBM

Figure 5 is a schematic of ball on polymer WLP structure with UBM. In this structure the solder ball is placed over RDL pad on a stack of polymer dielectric materials. Two-layers of dielectric materials (usually polyimide) are processed, named Polymer 1 and Polymer 2, respectively, to serve as passivation and redistribution layers. Redistribution copper traces connect final metal pads to solder balls with UBM incorporated. Polymer layer serves as stress buffer when thermal-mechanical stress is subjected due to thermal mismatch between PCB and silicon during temperature change. Detailed ball structure is shown in Figure 6.
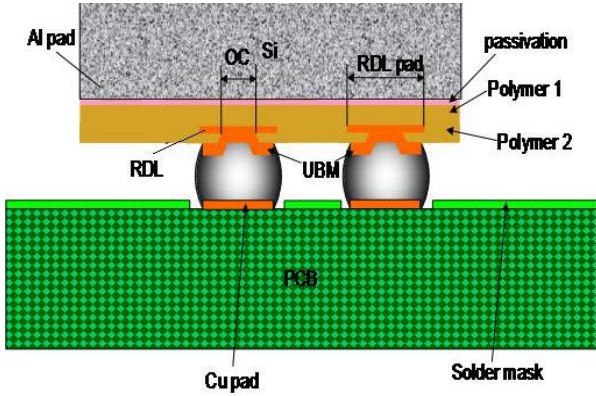
Figure 5 A schematic diagram of ball on polymer with UBM WLP
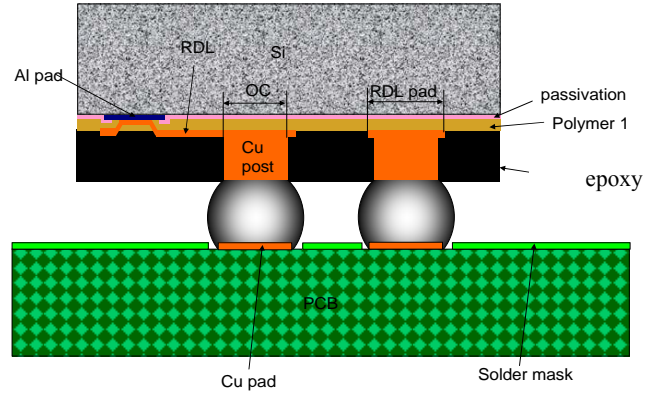

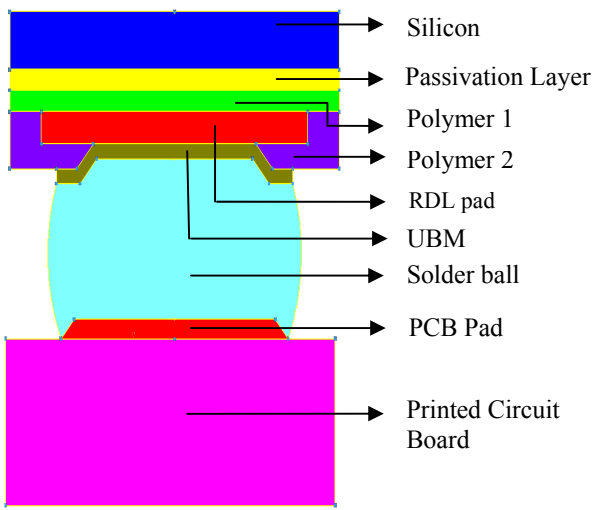Figure 7 A schematic diagram of Encapsulated copper post WLP

Figure 6 A schematic cross-section view of bump structure for WLP Structure C
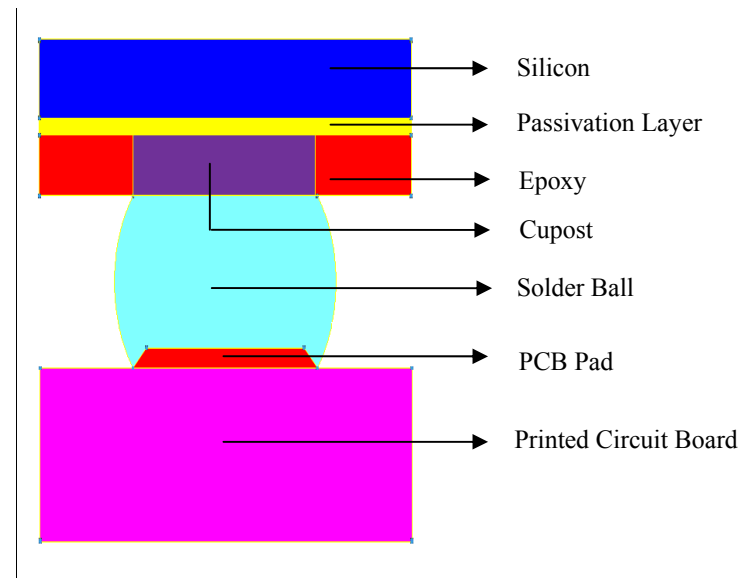

Figure 8 A schematic cross section view of bump structure for WLP Structure D

2.4 WLP Structure D: Encapsulated Copper Post WLP

In encapsulated copper post WLP technology, bond pads are redirected into an array of interconnects. They are in the form of electroplated copper posts instead of pads to provide enough confrontation for the active wafer surface to be encapsulated in low stress epoxy by transfer molding, exposing only the top portions of the posts where the solder balls will be attached, as shown in Figure 7. Detailed ball structure is shown in Figure 8.

In the following study, the ball pitch used for all structures is 0.5mm unless otherwise stated, and solder ball opening diameter on silicon side is fixed as 0.25mm. The PCB side is assumed non-solder mask defined. Other important geometrical dimensions of all four structures are shown in Table 2.

Table 2 Geometrical dimensions of WLP packages

WLP Structure	Dimensions (μm)			
	A	B	C	D
Silicon thickness	400	400	400	400
Solder ball diameter	310	310	310	310
Solder ball standoff height	240	240	240	240
Solder ball opening diameter	250	250	250	250
PCB pad diameter	250	250	250	250
PCB thickness	1000	1000	1000	1000

Wafer Passivation thickness	4	4	4	4
Pitch Size	500	500	500	500
UBM combined thickness	2.5	-	2.5	-
Epoxy/Copper post thickness	-	-	-	70
Polymer film 1 thickness	-	5	5	-
Polymer film 2 thickness	-	5	5	-

3. Finite Element Model

In the present study we consider only the equal array size of WLP packages in both directions. Thus one eighth model is created using symmetry condition. The top view of a WLP package is shown in Figure 9. Figure 10 shows finite element model of one eighth part of package. ANSYS 11.0 is used for all the finite element analysis. VISCO 107 linear element is used to mesh solder joint which allows using viscoplastic material properties. The Solid 45 element is used to mesh all other materials. In order to reduce the possible edge effect of PCB board on the outermost solder ball stress analysis, the PCB size in the model is extended at least 2.5 times of the package size, as shown in Figure 10. The boundary condition for the one eighth model involves applying symmetry boundary conditions on symmetric planes, the node at the origin is constrained so as to have zero displacement in all the three direction.
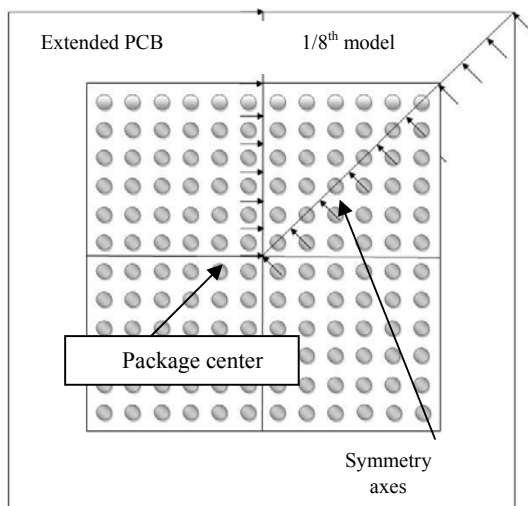

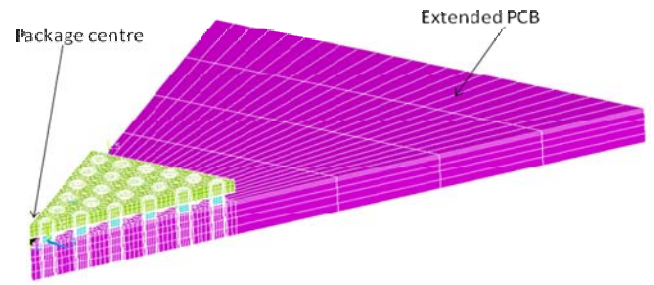
Figure 9. Top view of an equal array WLP package

Figure 10 One-eighth finite element model for WLP due to symmetry

Four WLP Structures A, B, C, and D are molded in detail and are shown in Figure 11. Figure 12 shows the experimental observations of failure mode at solder bulk due to fatigue on package side. In finite element models, a fixed-thickness layer (10μm) is created for each structure to extract damage parameter.

a) WLP structure A

b)WLP structure B
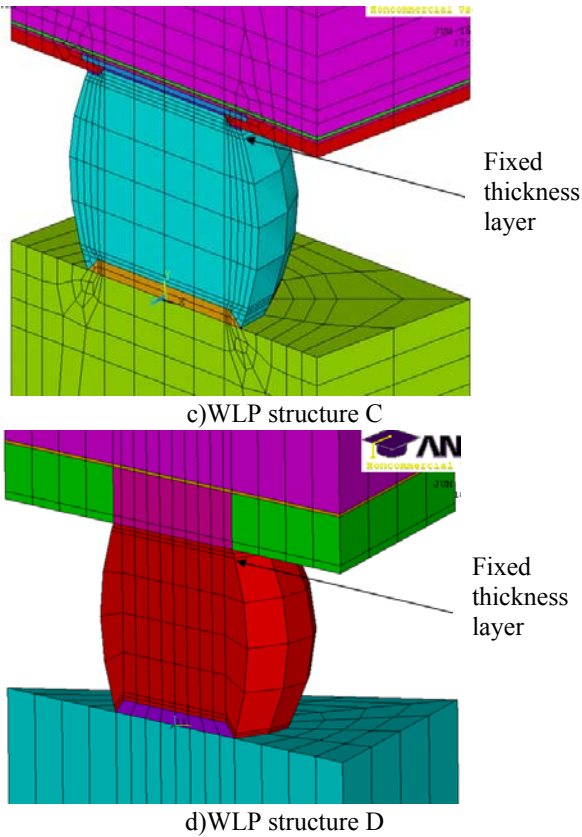
c)WLP structure C
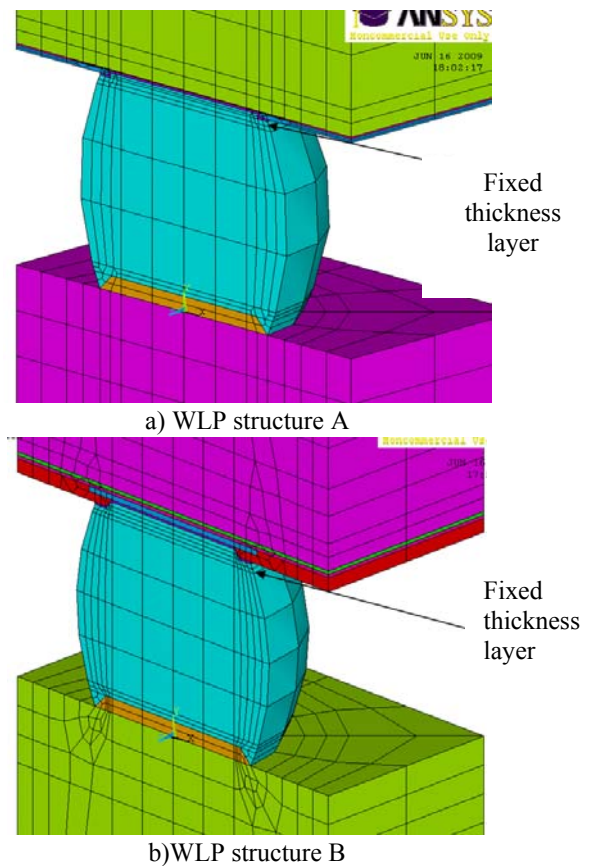
d)WLP structure D

Figure 11 Finite element models of various WLP structures
a). WLP Structure A; b). WLP Structure B; c). WLP
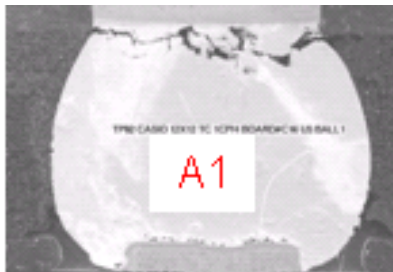Structure C; d). WLP Structure D

Figure 12 Solder bulk crack on package side due to fatigue

3.1 Material Properties

WLP packages are made of different materials. A summary of the materials used for analysis is shown in Table 3. All materials used in the analysis are modeled as linear elastic and the temperature dependency is taken into consideration whenever the glass transition temperature T_g is within the thermal cycling range of -45°C to 125°C. The PCB is fiber reinforced epoxies which makes the properties differ in out of plane direction. Orthotropic properties are therefore used for these materials.

Table 3 Material properties

Materials	Modulas of Elasticity (GPa)	Coefficient of Thermal Expansion (ppm/°c)	Poisson's ratio
Silicon	130	2.6	0.278
Passivation	105	11	0.24
UBM	50	16	0.35
Aluminum Pad	69	24	0.32
RDL pad	130	16.8	0.34
Epoxy	14	20	0.24
Polymide	1.2	52	0.34
Polymer 1	1.2	52	0.34
Polymer 2	1.2	52	0.34
Cu Post	130	16.8	0.34
Solder Ball	50	24.5	0.35
Pcb pad	130	16.8	0.34
PCB	25	16	0.39

The solder joint used for the analysis is SAC305 alloy. This alloy is modeled as rate-dependant viscoplastic material property using ANAND model (Anand 1985) [5]. The Anand model in commercial software ANSYS has been used here to characterize the rate-dependent creep behavior of solder alloys at varying temperatures. In Anand model, the flow equation is,

$$d^p = A e^{-\frac{Q}{R\theta}} \left[\sinh\left(\zeta \frac{\sigma}{s}\right) \right]^{\frac{1}{m}}$$

$$s = \{h_0 (|B|)^a \text{sgn}(B)\} d^p$$

$$B = 1 - \frac{s}{s^*}$$

$$s^* = s\left[\frac{d^p}{A} e^{\frac{Q}{R\theta}}\right]^n \qquad (1)$$

where, d = effective inelastic deformation rate,
σ = the effective Cauchy stress,
s = the deformation resistance,
s* = the saturation value of deformation resistance,
ś = the time derivative of deformation resistance,
θ = the absolute temperature.

Darveaux (1995, 2000) [7] [8] gave the nine material constants in Equation (1) for eutectic solder alloys. This has led the Anand model very popular in solder joint reliability modeling. For SnAgCu alloys, this paper uses the material constants given by Reinkainen et al. (2005) [11]. He has fitted 9 constants for SAC305 alloy. Table 4 lists the Anand's model constants used in SAC 305 alloy.

Table 4 Material parameters of viscoplastic Anand model
(Reinkainen et al., 2005) [11]

Constant	Constant Value
s_0, MPa	1.3
Q/R, K	9000
A, sec^{-1}	500
ξ	7.1
m	0.3
h_0, MPa	5900

s^, MPa	39.4
n	0.03
α	1.5

3.2 Loading Condition

Stress free initial temperature is important consideration before subjecting any package to loading profile (Fan *et al.*, 2006) [9]. It is temperature of a material corresponds to the temperature at which the material has either been cured or assembled. There are three commonly used initial stress-free temperature conditions. One is the solidus temperature of solder material (e.g., for SAC305, this temperature is 217°C). This condition considers that the solder joints start to provide mechanical support as soon as the solder material is solidified during the reflow process. The second one is the room temperature as initial stress-free (e.g. 25°C). This assumes that the shipping and storage time is sufficient to relax all the residual stresses in solder joints from the assembly process. The last one uses the high dwell temperature of thermal cycle or operating conditions (denoted as Tmax, e.g. =125°C for thermal cycling from -45°C to 125°C). This assumes that after several thermal cycles, the package reaches a stabilized cyclic pattern where the lowest stresses are seen at the end of the high temperature dwell period.
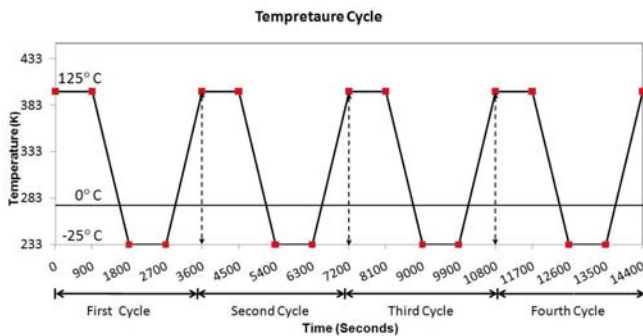

Figure13 Temperature cycle used for simulation

In this analysis, we have used thermal cycle condition -40°C to 125°C to ensure a reliable package performance. Figure shows a loading profile for simulation which includes four cycles, each cycle is 60 minutes with 15 minutes ramp up and down time and 15 minutes of dwell time at -40°C and 125°C. According to previous studies, viscous material, used for solder ball, readjust the stress state and reach 'a near stress free' at high dwell temperature after few cycles. It also indicates that the stabilized values of strain or strain energy density per cycle are independent of the initial stress free temperature setting and results showed that the stabilization happened within the first cycle (Fan *et al.*, 2006) [9].

3.3 Analysis approach

There are many methods to evaluate solder joint reliability, e.g., stress based, plastic/creep strain based, energy based, and damage accumulation based. In this paper, the analysis is based on damage accumulation method. Usually per-cycle inelastic strain (or creep strain) or inelastic

strain energy density is used as damage metrics to evaluate solder joint reliability. To prevent any mesh dependency and stress singularity effect at geometry edge, Darveaux (1995, 2000) [7-8] has used a solid thin layer of elements near package/solder interface for volume averaging. All four WLP structures are modeled with a 10μm thin disk with two layers of element as shown in Figure 14.

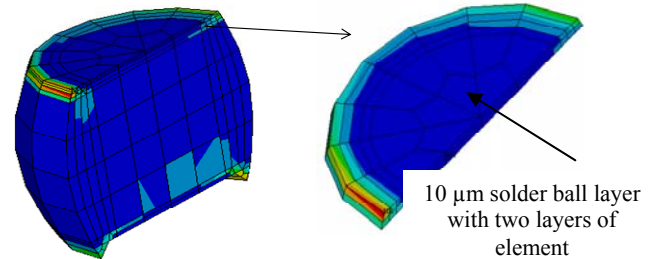10 μm solder ball layer with two layers of element

Figure 14 Volume averaging on a fixed thickness layer

The volume averaged inelastic energy density is defined as over the thin disk of two layered element as follows,

$$\Delta W_{ave} = \frac{\Sigma \, \Delta W \, V}{\Sigma V} \qquad (2)$$

where,

ΔW_{ave} = Average viscoplastic strain energy density accumulated per cycle for interface element

ΔW = Average viscoplastic strain energy density accumulated

V = Volume of each element

This equation gives accumulated inelastic energy density per cycle and accumulation comes from all four time periods during each cycle, i.e., ramp up and down and dwell at extreme high temperature and extreme low temperature.

3.4 Important Observations

1) Results show that the maximum damage occurs in the diagonally outer most solder ball, which is also known as the critical solder ball.
2) We have used four complete cycles of thermo mechanical loadings. It has been found that the averaged inelastic strain energy accumulation per cycle is approximately same for all cycles.

Therefore, for analysis purpose, the accumulated damage, e.g. inelastic energy density, is calculated only for critical solder ball in the following from the first cycle result.

4. Modeling Results-Parametric Study
4.1 Effect of Pitch Size

Figure 15 shows the inelastic strain energy density for two pitches, 0.4mm and 0.5mm, respectively. When the pitch decreases, the solder joint fatigue life is improved.
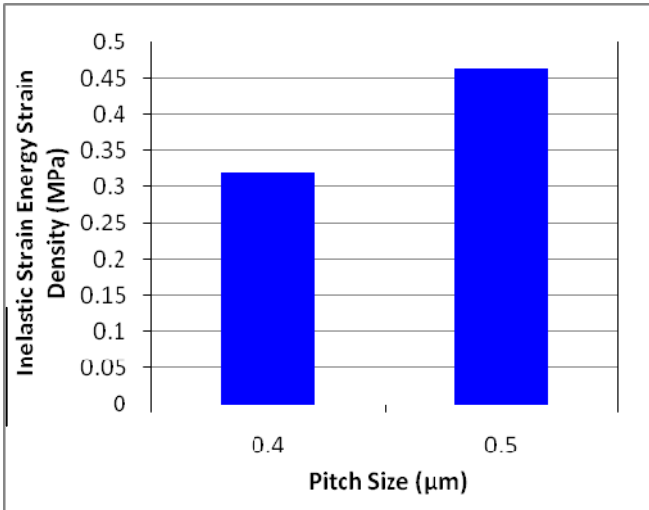
Figure 15 Effect of pitch size

4.2 Effect of Array Size

With increasing array size, inelastic strain energy density continues to increase, therefore fatigue life continues to decreases. Figure 16 shows the results from 6×6 array size to 12×12 array.
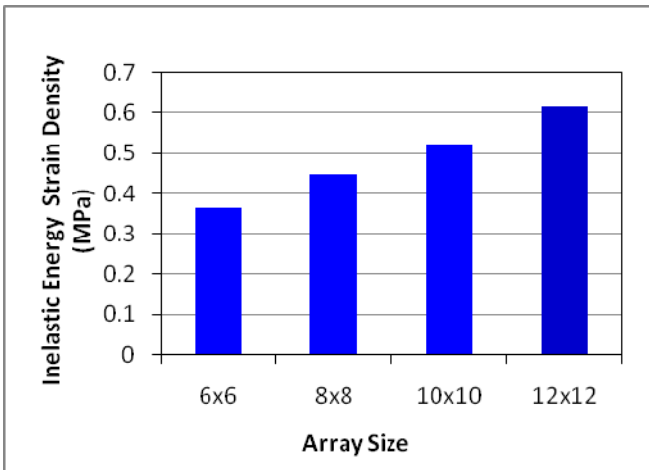

Figure 16 Effect of array size

4.3 Effect of Solder Ball Diameter

By keeping other parameters same, increasing solder ball diameter will increase inelastic strain energy density, and therefore decreases fatigue life under thermal cycling. Figure 17 shows inelastic energy density results for 220µm, 300µm, and 350µm diameters, respectively.
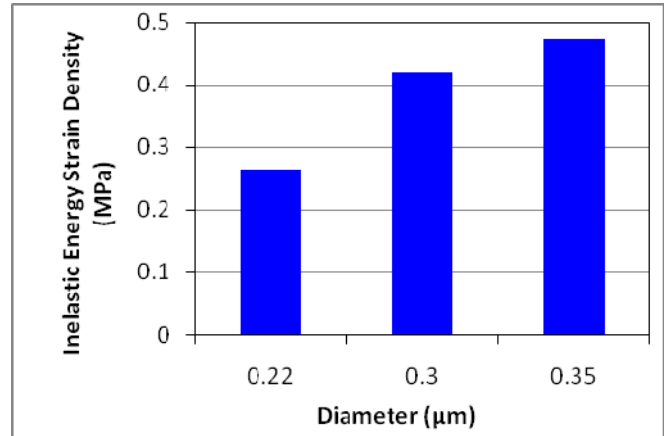

Figure 16 Effect of solder ball diameter

4.4 Effect of Solder Ball Opening Diameter

A larger solder ball opening diameter increases the total contact/interface area, and therefore it takes a longer time for solder ball crack propagations throughout contact interface. Figure 18 shows increasing die size opening diameter from 0.250µm to 0.280µm increases solder joint reliability. It becomes obvious that increasing the contact area-solder ball opening diameter is the most direct way to improve the solder joint reliability because failures often take place at solder bulk near solder ball/package interface.
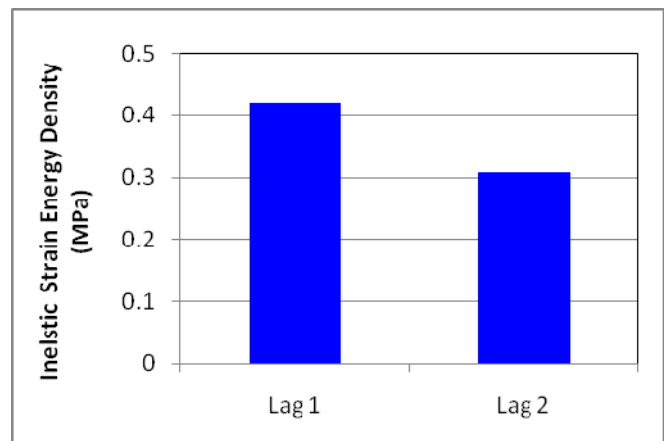

Figure 18 Effect of solder ball opening diameter

4.5 Effect of UBM

Figure 19 shows comparison of inelastic strain energy density of two structures B and C. The difference between two structures is that structure B does not have UBM layer. Results indicate that the UBM layer has slightly beneficial effect on thermo-mechanical performance of solder joint reliability.
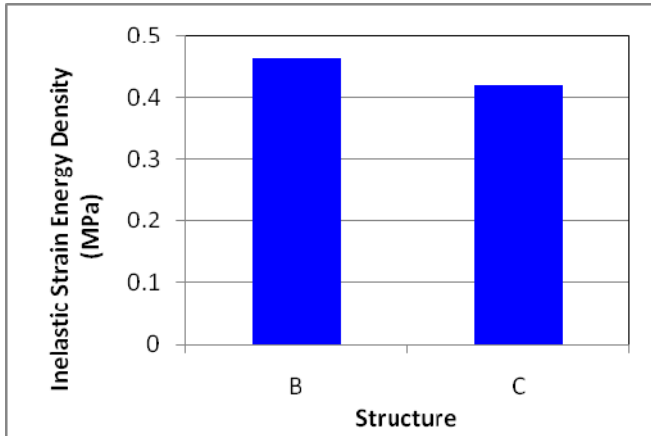
Figure 19 Effect of UBM

4.6 Effect of Passivation Layer

Thermal cycling finite element modeling results show insignificant effect of passivation layer in both structures B and C. Figure 20 shows that eliminating passivation layer in finite element model present good results for both Structure B and C.
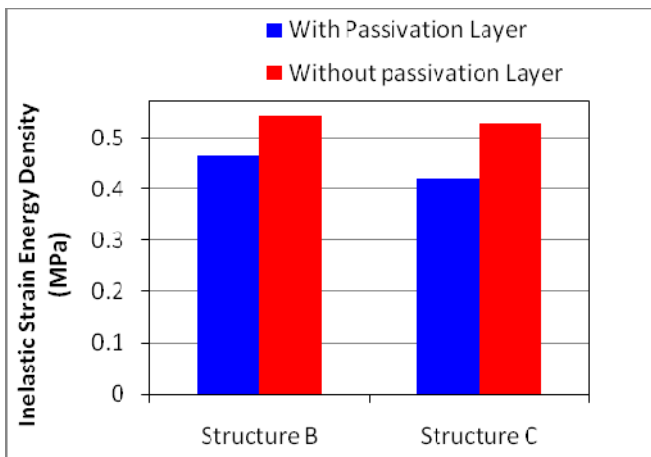

Figure 20 Effect of Passivation Layer

4.7 Effect of Material Properties of Polymer Film 1

Polyimide film is usually used for polymer 1 and 2 in WLP Structures B and C. From Table 3, it can be seen that polyimide is very compliant with a Young's modulus of 1.2GPa, and a coefficient of thermal expansion of $52\times10^{-6}/°C$ respectively. The extreme compliance of polyimide film is often attributed to be the reason for thermal-mechanical performance improvement in solder joints.
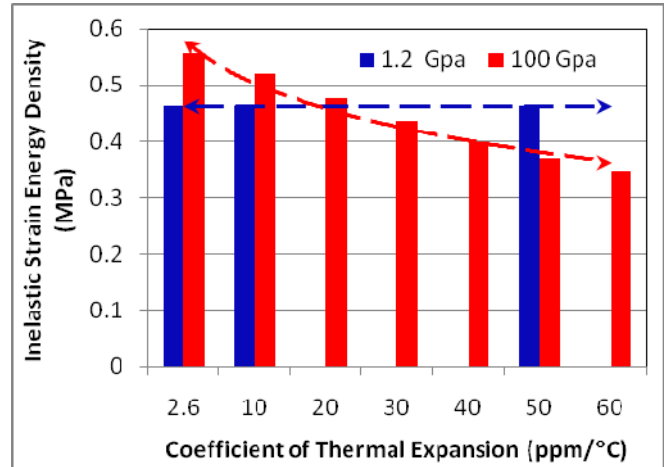

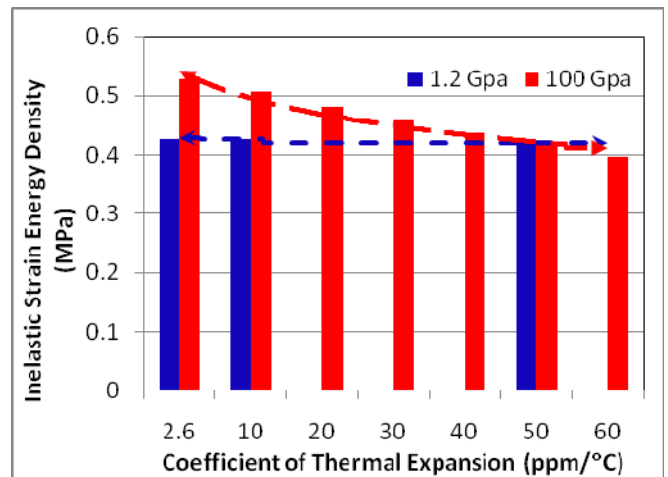Figure 21 a) Effect of Modulas of Elasticity and CTE of Polymer film in Structure B

Figure 22 b) Effect of Modulas of Elasticity and CTE of Polymer film in Structure C

A parametric matrix study is performed to understand the effects of Young's modulus and CTE of the film, as shown in Figures 21 (a) and (b), respectively. When the modulus is 1.2GPa, which means that film is extremely compliant, the CTE of the film has no effect on solder joint behavior. However, when film modulus is 100GPa, solder joint stress decreases significantly with the increasing of film CTE. When the CTE is above $50\times10^{-6}/°C$, solder joint stress is even lower than that the case with the film Young's modulus of 1.2GPa. Such results indicate that the stress buffer effect can be realized either with extreme compliant material or 'hard' material with relatively large CTE. For a very soft film, solder joint stresses are relieved due to large deformation of film. For a hard film with larger CTE, the overall CTE of the combined silicon/film structure increases, therefore, the thermal mismatch with PCB is reduced. Fig. 21 b) show the effects of material properties of polymer film 1 for Structure C, and same conclusion can be reached. Figure 21 c) shows comparison of solder joint reliability of both structures at higher modulas of elasticity of polymer film. It indicates solder joint reliability decreases for UBM

structure at higher CTE. It means Structure B has better reliability at higher modulas of elasticity and CTE.
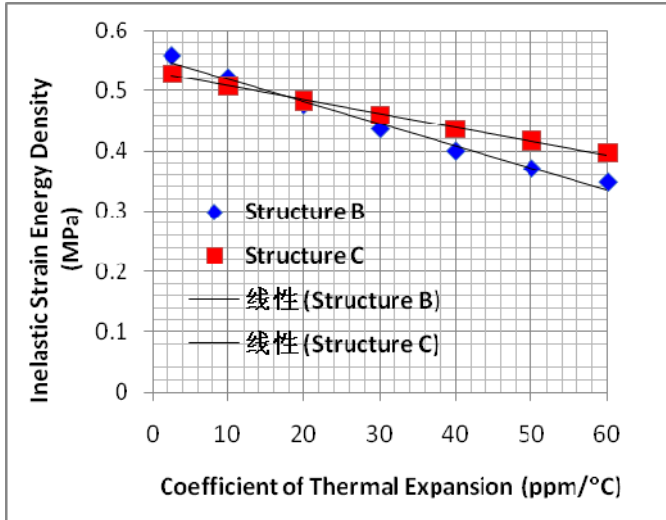

Figure 21 c) Comparison of solder joint reliability of both structures at higher Modulas of Elasticity of Polymer film

These results show that there might be an optimal point for both CTE and modulus to achieve the maximum benefit for solder joint reliability improvement. By optimizing polymer material properties, Structure B and C WLP reliability can be further enhanced.

4.8 Effect of Thickness of Polymer Thickness

Increasing polymer thickness in both structures B and C improves solders joint reliability, as shown in Figure 22. (Leg 1 film thickness < Leg 2 film thickness).
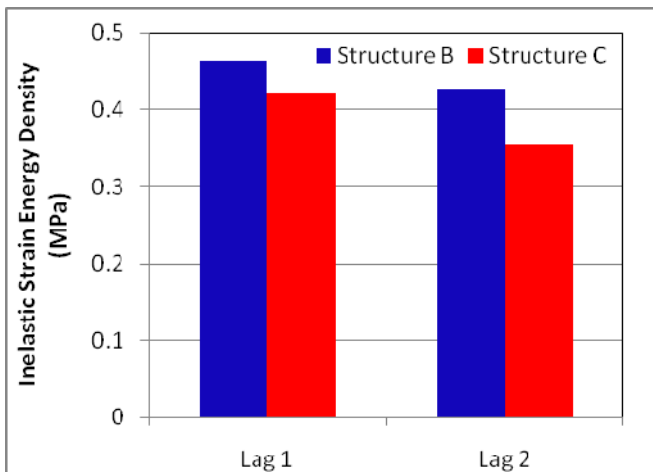

Figure 22 Effect of Polymer Thickness

4.9 Effect of Epoxy

The CTEs of the encapsulated epoxy and copper post in WLP Structure D are $20\times10^{-6}/°C$ and $17\times10^{-6}/°C$, respectively, which are much greater than silicon's. Therefore, the effective CTE of the encapsulated silicon increases effectively, which reduces the thermal mismatch

with the PCB. As a result, solder joint stresses are reduced. In order to understand the effect of material properties of epoxy, a parametric study is performed, as shown in Figs. 23 and 24, respectively. When the CTE of the epoxy is kept at $20\times10^{-6}/°C$, the modulus of epoxy has nonlinear relationship with ΔW. It seems an optimal value is around 70GPa for the lowest solder joint stress. On the other hands, in Fig. 24, it can be seen that further increasing epoxy CTE from $20\times10^{-6}/°C$ to $40\times10^{-6}/°C$ will reduce stresses in solder joint, but stress will not go down further from $40\times10^{-6}/°C$ to $60\times10^{-6}/°C$. These results show that there might be an optimal point for both CTE and modulus to achieve the maximum benefit for solder joint reliability improvement. By optimizing epoxy material properties, Copper Post WLP reliability can be further enhanced.
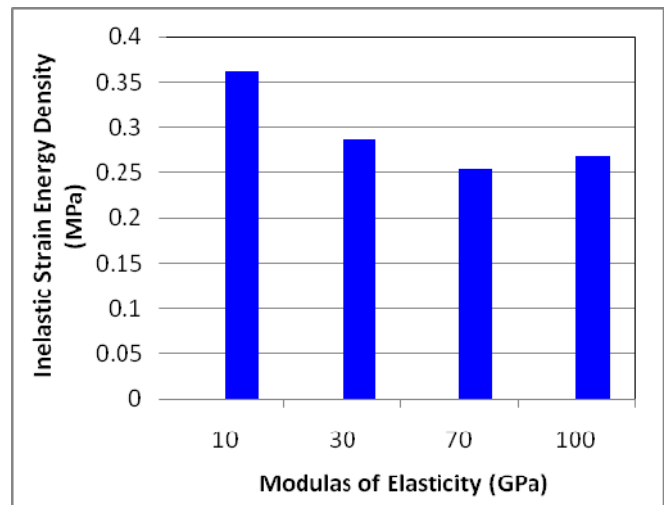

Figure 23 Effect of epoxy modulus in WLP Structure D (CTE=20ppm/°C)
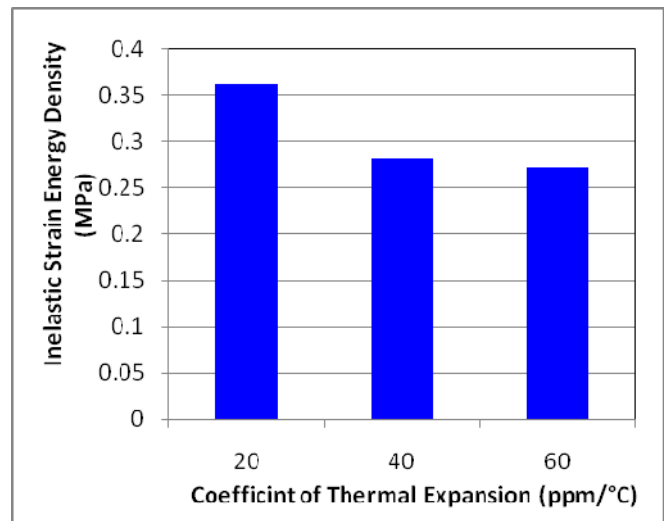

Figure 24 Effect of epoxy CTE in WLP Structure D (E=14GPa)

4.10 Effect of Material Properties of PCB

Thermal-mechanical stresses developed in solder joints are induced by the thermal mismatch between PCB and

silicon. Lowering the CTE of PCB can also reduce the stresses in solder joints. Figure 25 shows the results of inelastic strain energy density for three set of PCB CTEs. When low CTE PCB core material is used, the fatigue life can be increased greatly. It has been demonstrated that a polymer film layer between solder balls and silicon with a larger CTE can increase the overall effective CTE of silicon, and thus reduce the thermal mismatch with PCB. Similar concept can be developed at PCB side to include a layer of material between PCB and solder balls. The detailed studies will be reported separately.
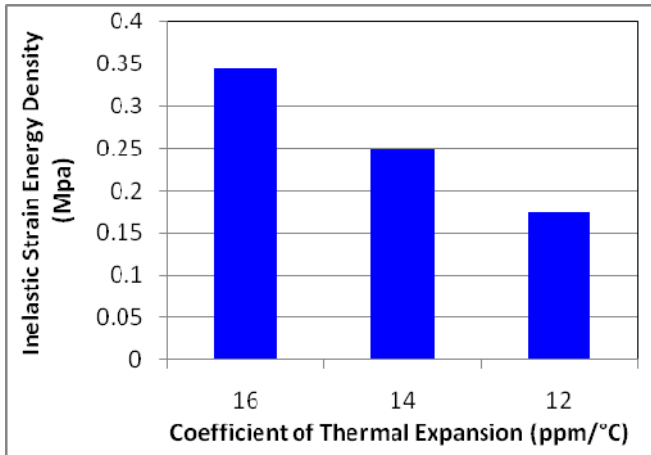

Fig.ure 25 Effect of PCB CTE on solder joint reliability

4.11 Effect of WLP Structure

Fig. 26 shows the per-cycle inelastic strain energy densities for four WLP Structures A, B, C, and D, respectively, for a 12×12 array packages with 0.5mm pitch.
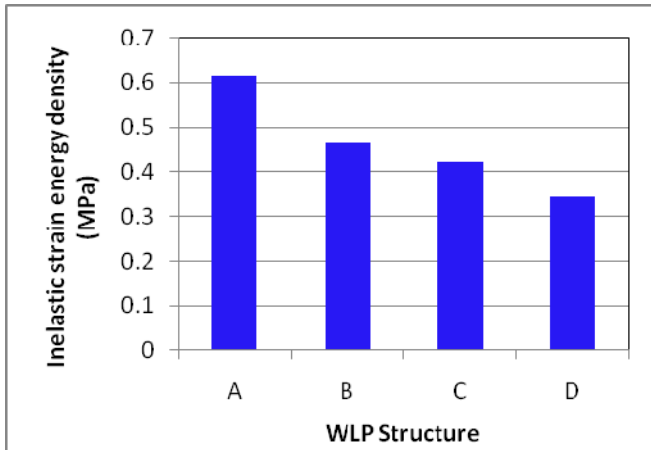

Figure 26 Effect of WLP structure

Compared to the Structure A, all other three Structures B, C and D showed more than 30% reduction in the accumulated inelastic strain energy density per cycle. This means that, with the incorporation of a dielectric polymer film between solder ball and silicon, or an encapsulated copper post layer, the stresses in solder joints can be reduced significantly compared to a 'rigid' connection in Structure A. Structure D with encapsulated copper post showed the best

performance. Experimental data have shown that Structure A WLPs can survive only up to 6x6 array size while all other three structures can pass thermal cycling reliability requirement up to 12×12 array sizes (Fan *et al.*, 2009) [2]. The finite element modeling results are consistent with experimental observations.

4.12 Solder Ball Damage Map

The inelastic energy dissipation plot is given by Figure 27. It is seen that the corner solder ball shows the highest energy dissipation and therefore the largest damage accumulation during temperature cycling. The energy dissipation decays rapidly both along die edge and diagonal direction towards package center. Results show if the corner solder balls are not electrically connected the WLP reliability would be greatly enhanced. This agrees well with the test results.
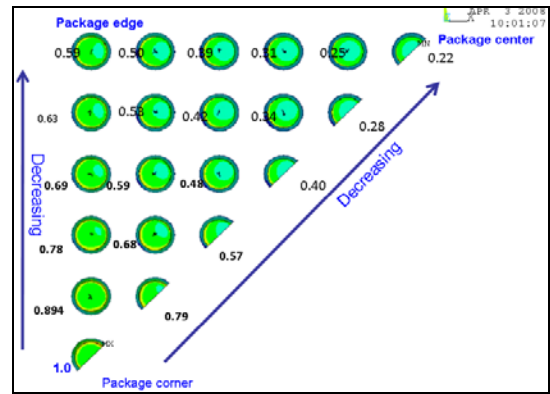

Figure 27 Inelastic Energy Density Contour for Corner Solder Joint

In order to understand the locations of solder joint crack initiation, von Mises stress plot of the solder joints are presented (Figure 28). It is seen that there is stress concentration at both sides for each solder ball. This explains the observation of cracks initiation from both sides of the solder joint. Furthermore, it is seen that the stress is higher at the inner side. This suggests that crack initiates first from inner side. This observation agrees with the findings from the failure analysis.
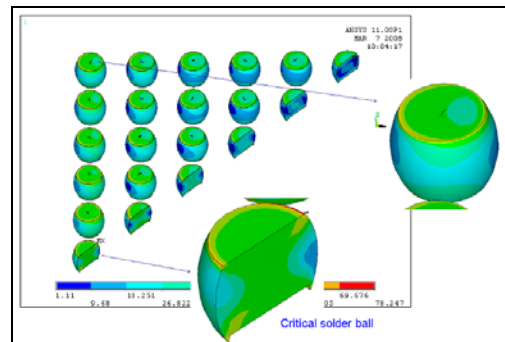

Figure 28 von Mises Stress in Solder Balls for identifying the Critical Ball

5. Experimental Validations [12]

To assess the wafer level package capability and technology limit, the following parameters are considered in experimental study to correlate with simulation results (Rahim *et al.* 2009) [12].

1. Different WLP structures
2. Ball pitches of 0.5 and 0.4 mm.
3. Array sizes of 12×12 and 10×10

5.1 Array Size

A comparison of failure data for 10×10 and 12×12 array sizes for WLP-C is shown in Table 5. It is observed that WLP-C, 10×10 array has 20% longer fatigue life than 12×12 array. In this case the ratio of WLP size between 12×12 and 10×10 array is 1.2. It appears that the fatigue life is inversely proportional to the package size.

Table 5 Normalized Characteristic Life for 12×12 and 10×10 Array WLP

Array Size	12x12	10x10
Characteristic life	1	1.2

5.2. WLP Ball Pitch

12×12 array WLPs with 0.5 and 0.4mm pitches are tested. WLP fatigue lives are compared against each other (Table 6). It is observed that 0.4mm pitch has 30% longer fatigue life than 0.5mm.

Table 6 Normalized Characteristic Life for 0.5mm and 0.4mm Pitch WLP

Pitch	0.5 mm	0.4 mm
Characteristic Life	1	1.3

Conclusions

Four different WLP structures are studied to investigate the effect of WLP structures on solder joint reliability with a combined modeling, test and failure analysis approach. These four WLP structures are Bump on I/O with and without RDL, Bump on Polymer with UBM, Bump on Polymer without UBM, and Encapsulated Copper Post. Although Ball on I/O WLP structure is limited for the application in small array packages, it has been used as a benchmark here for the analysis. Finite element models for these WLP structures have been created and analyzed. Results showed that Ball on Polymer with and without UBM, as well as Copper Post WLPs had a great improvement in thermo-mechanical reliability performance over the Bump on I/O WLPs.

Thermo-mechanical reliability of solder joints of WLP packages can also be improved by optimizing ball geometry and array size and pitch. The more compliant solder ball is, the greater thermo-mechanical reliability is achieved. Therefore, reducing individual solder ball volume or using more compliant materials such as polymer cored solder balls will improve reliability performance. As solder balls become the weakest link during thermal cycling, increasing the contact area-solder ball opening diameter is the most effective way to improve the solder joint reliability. Also, small array size and lower pitch size has better reliability compare to higher array size and pitch size.

Materials also play important roles in enhancing solder joint reliability. In Ball on Polymer WLP structure, polymer film between silicon and solder balls creates a 'cushion' effect to reduce the stresses in solder joints. Such cushion effect can be achieved either by an extremely compliant film or a 'hard' film with large coefficient of thermal expansion. In the later case, the reduction of solder joint stresses is due to the overall increase of the combined film/wafer effective CTE. It has been found that a 'hard' layer with a large CTE can reduce solder joint stress beyond a compliant film. This has been validated by encapsulated Copper Post WLP structure, which showed the best performance on all four structures in terms of solder joint reliability.

The crack is in bulk solder at package side. The cracks initiate from both sides of the solder joint. The cracks propagate from edge toward the center of the solder ball. The corner balls are most susceptible to solder joint failures. Based on test data, making corner balls electrically not connected improves the WLP reliability by 20%. It is concluded that for a given ball array size, smaller pitch gives better solder joint life.

References

1. Fan, X.J., Han, Q., 2008. "Design and reliability in wafer level packaging," *Proc of IEEE 10th Electronics Packaging Technology Conference (EPTC)*, pp. 834-841, 2008
2. Fan, X.J., Liu, Y. 2009. "Design, Reliability and Electromigration in Chip Scale Wafer Level Packaging," *ECTC Professional Development Short Course Notes*.
3. Reche, J.J.H., and Kim, D.H. 2003. "Wafer level packaging having bump-on-polymer structure, Microelectronics Reliability," 43, pp. 879-894.
4. Kim, D.H., Elenius, P., Johnson, M., and Barraett, S. 2002. "Solder joint reliability of a polymer reinforced wafer level package," *ECTC*.
5. Anand, L., 1985. "Constitutive equations for hot working of metals," *J. Plasticity*, 1, pp. 213-231.
6. Bumping Design Guide, [online], Available: http://www.flipchip.com/
7. Darveaux, R., Banerji, K., Mawer, and Dody, G. 1995. Reliability of plastic ball grid array assembly, Ball Grid Array Technology, Lau, J. ed, McGraw-Hill, New York
8. Darveaux, R. 2000. "Effect of simulation methodology on solder joint crack growth correlation," 2000, *Proc. ECTC*.
9. Fan, X. J., Pei, M., and Bhatti, P.K. 2006. "Effect of finite element modeling techniques on solder joint fatigue life prediction of flip-chip BGA packages," *Proc. Of IEEE Electronic Components and Technology Conference (ECTC)*, May 30-June 2, San Diego, CA.
10. Kawahara, T. 2002. SuperCSPs, IEEE Transactions on Advanced Packaging, v.23, No. 2.
11. Reinikainen, T.O, Marjamäki, P., Kivilahti, J.K. 2005. "Deformation characteristics and microstructural evolution of SnAgCu solder joints," *EuroSimE*.

12. Rahim, M.S.K., Zhou, T., Fan, X.J., Rupp, G. 2009. "Board level temperature cycling study of large array wafer level packages," *Proc of Electronic Components and Technology Conference (59th ECTC)*, pp. 898-902.

13. Syed, A. 2001. "Predicting solder joint reliability for thermal, power, & bend cycle within 25% accuracy," *51st ECTC*, pp. 255-263.